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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,809	01/09/2002	Bruce Michael Cassidy	IBMS.040US01 (0543)	5058

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Chambliss, Bahner & Stophel, P.C.
1000 Tallan Building
Two Union Square
Chattanooga, TN 37402

EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,809	CASSIDY, BRUCE MICHAEL	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *56-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *56-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 56-68 are presented for examination.

Claim Objections

2. Claim 56 is objected to because of the following informalities: "the retrieved host command" (line 7) should be changed to "the retrieved host commands" to be consistent with "commands" being cited earlier in the claim. Appropriate correction is required.

3. Claim 65 is objected to because of the following informalities: "a the peripheral device" (line 5) should be changed to "the peripheral device" to be consistent with "commands" being cited earlier in the claim. Appropriate correction is required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Claim 64 recites the limitations "the peripheral device processor further comprises *a peripheral device means*, operatively coupled via a bus means to host memory means, the peripheral device means including *peripheral device processing* for controlling operation of the peripheral device means". Therefore, the "*peripheral device means*" and "*peripheral device processing*" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet,

even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 56-68 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter "***discrete host***" which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. Claim 64 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter "the peripheral device

processor further comprises *a peripheral device means*, operatively coupled via a bus means to host memory means, the peripheral device means including *peripheral device processing* for controlling operation of the peripheral device means" which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 66-67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

First, claim 66 depends on claim 64 and recites the limitation of "retrieving, using the host messaging unit, the host commands from host memory without adding process loading to the host processor of the discrete host". This limitation has already been cited in claim 64, thus the two claims are identical.

Second, claims 66 and 67 recite "The method of claim 64", however, claim 64 is not a method claim. And according to the claim language, it is consistent that the claims should have depended on method claim 65 instead of claim 64. Therefore, the Examiner treated the claims as they depend on claim 65. However, if Applicant believes that the claims still depend on claim 64, the reference(s) and/or arguments used in rejecting the claims are applied in addition to the reference(s) used in rejecting claim 64 if needed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 56-59 and 64 are rejected under 35 U.S.C. 102(e) as being anticipated by Micalizzi, Jr. et al. (6,564,271) (hereinafter Micalizzi).

As to claim 56, Micalizzi teaches a system providing peripheral component device interconnection, comprising: a peripheral device processor (processor 122 and associated circuitry) for controlling operation of the peripheral device (adapter board 116 or I/O devices 132-134) (Fig. 1); and a host messaging unit (inbound logic 202 and associated circuitry), coupled to the peripheral device processor, but separate from the peripheral device processor (Figs. 2-3), the host messaging unit retrieving host commands (I/O command blocks IOBCs) from a host memory (e.g. request queue 110) of a discrete host (host 102) without adding process loading to the peripheral device processor (processor 122 only needs to read the IOCBs from the adapter IOCB buffer area instead of having to set up the transfer of the IOCBs from the host to the adapter RAM 138. The IOCBs are automatically offloaded from RAM 138, allowing processor 122 to process responses at a higher rate) (col. 3 lines 58-67, col. 7 lines 35-48 and col. 9 lines 26-48), validating the retrieved host command (checking for error) (col. 7 lines 9-20) and asynchronously signaling a successful transfer of the host commands from host

memory to the host messaging unit (inbound logic 202 de-queues the request queue 110 and controls the out-pointer 404 to signal successful receiving of the commands) (Fig. 3 and col. 5 lines 60-67).

As to claim 57, Micalizzi further teaches the host messaging unit retrieves host commands from a host memory of a discrete host without adding process loading to a host processor of the discrete host (col. 6 lines 48-67).

As to claim 58, Micalizzi further teaches the host messaging unit provides signaling between the peripheral device and the discrete host asynchronous to operation of the discrete host and the peripheral device (col. 6 line 36 to col. 7 line 48).

As to claim 59, Micalizzi further teaches the host messaging unit is disposed external to the peripheral device and provides signaling between a plurality of peripheral devices (e.g. I/O devices 132-134) and the discrete host (Fig. 1 and col. 3 lines 58-67), the operation of the host messaging unit being asynchronous to operation of the discrete host and the peripheral devices (col. 6 line 36 to col. 7 line 48).

As to claim 64, Micalizzi further teaches the peripheral device processor further comprises a peripheral device means (processor 122), operatively coupled via a bus means (e.g. bus 114) to host memory means, the peripheral device means including peripheral device processing for controlling operation of the peripheral device means (col. 4 lines 1-7) and wherein the host messaging unit further comprises host messaging means (e.g. inbound logic 202), coupled to the peripheral device processing means, but separate from the peripheral device processing means (Figs. 2-3), the host messaging means retrieving the host commands from the host memory means of a discrete host

means without adding process loading to the host processing means or the peripheral device processing means (processor 122 only needs to read the IOCBs from the adapter IOCB buffer area instead of having to set up the transfer of the IOCBs from the host to the adapter RAM 138. The IOCBs are automatically offloaded from RAM 138, allowing processor 122 to process responses at a higher rate) (col. 3 lines 58-67, col. 7 lines 35-48 and col. 9 lines 26-48), validating the retrieved host command (checking for error) (col. 7 lines 9-20) and asynchronously signaling a successful transfer of the host commands from host memory means to the host messaging means (inbound logic 202 de-queues the request queue 110 and controls the out-pointer 404 to signal successful receiving of the commands) (Fig. 3 and col. 5 lines 60-67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Micalizzi, Jr. et al. (6,564,271) (hereinafter Micalizzi) in view of Nelson et al. (5,574,863) (hereinafter Nelson).

As to claim 65, Micalizzi teaches a method of servicing a peripheral component interconnect device, comprising: providing a host messaging unit (inbound logic 202 and

associated circuitry) operatively disposed between a discrete host (host 102) having a host processor (processor 104) and a peripheral device processor (122) for providing a signal interface that operates asynchronously with respect to the operation of the host processor and the peripheral device (Figs. 1-3); retrieving, using the host messaging unit, the host commands from host memory without adding process loading to the peripheral device processor (processor 122 only needs to read the IOCBs from the adapter IOCB buffer area instead of having to set up the transfer of the IOCBs from the host to the adapter RAM 138. The IOCBs are automatically offloaded from RAM 138, allowing processor 122 to process responses at a higher rate) (col. 3 lines 58-67, col. 7 lines 35-48 and col. 9 lines 26-48); validating the retrieved host command at the host messaging unit (checking for error) (col. 7 lines 9-20); and clearing the host memory to allow the discrete host to infer that the host command has been read by the host messaging unit (inbound logic 202 de-queues the request queue 110 and controls the out-pointer 404 to signal the host that the command has been read) (Fig. 3 and col. 5 lines 60-67); and providing the host command to the peripheral device processor for processing by the peripheral device processor (col. 9 lines 26-40). Micalizzi further teaches polling by the host messaging unit to detect when the host processor has loaded a new host command into host memory coupled to the host processor (col. 6 lines 48-56). However, Micalizzi does not explicitly disclose signaling the host messaging unit when there is a new message loaded in the memory. Nelson teaches in addition to polling, using interrupt signaling to notify when there is new message in the mailbox (after a requesting agent writes message into the mailbox, generating an interrupt signal to notify the reply agent that a message exists in

the mailbox for the reply agent to read) (col. 4 lines 43-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the interrupt signaling as taught by Nelson in the system of Micalizzi to provide additional robustness and reliability of communication between agents in the case of failure of one method or the other (col. 4 line 66 to col. 5 line 2).

As to claim 66, Micalizzi further teaches retrieving, using the host messaging unit, the host commands from host memory without adding process loading to the host processor of the discrete host (col. 6 lines 48-67).

As to claim 67, Micalizzi does not explicitly disclose providing a clock to control the initiation of the retrieval of the host command from the host memory at predetermined intervals. Nelson further teaches providing a clock to control the initiation of the retrieval of new message from the host memory at predetermined intervals (lines 58-66 and col. 7 lines 51-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement providing a clock to control the retrieval of new message at predetermined intervals as taught by Nelson in the system of Micalizzi to enhanced reliability to the communication process and system.

As to claim 68, Micalizzi teaches an article of manufacture comprising: a program storage medium readable by a computer, the medium tangibly embodying one or more programs of instructions executable by the computer to perform operations for reducing bus transfer overhead between a host processor and a peripheral component interconnect device processor, the operations comprising: providing a host messaging unit (inbound logic 202) operatively disposed between a discrete host (host 102) having a host

processor (processor 104) and a peripheral device processor (processor 122) for providing a signal interface that operates asynchronously with respect to the operation of the host processor and a the peripheral device (Figs. 1-3); retrieving, using the host messaging unit, the host commands from host memory without adding process loading to the peripheral device processor (processor 122 only needs to read the IOCBs from the adapter IOCB buffer area instead of having to set up the transfer of the IOCBs from the host to the adapter RAM 138. The IOCBs are automatically offloaded from RAM 138, allowing processor 122 to process responses at a higher rate) (col. 3 lines 58-67, col. 7 lines 35-48 and col. 9 lines 26-48); validating the retrieved host command at the host messaging unit (checking for error) (col. 7 lines 9-20); and clearing the host memory to allow the discrete host to infer that the host command has been read by the host messaging unit (inbound logic 202 de-queues the request queue 110 and controls the out-pointer 404 to signal the host that the command has been read) (Fig. 3 and col. 5 lines 60-67); and providing the host command to the peripheral device processor for processing by the peripheral device processor (col. 9 lines 26-40). Micalizzi further teaches polling by the host messaging unit to detect when the host processor has loaded a new host command into host memory coupled to the host processor (col. 6 lines 48-56). However, Micalizzi does not explicitly disclose signaling the host messaging unit when there is a new message loaded in the memory. Nelson teaches in addition to polling, using interrupt signaling to notify when there is new message in the mailbox (after a requesting agent writes message into the mailbox, generating an interrupt signal to notify the reply agent that a message exists in the mailbox for the reply agent to read) (col. 4 lines 43-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the interrupt signaling as taught by Nelson in the system of Micalizzi to provide additional robustness and reliability of communication between agents in the case of failure of one method or the other (col. 4 line 66 to col. 5 line 2).

Allowable Subject Matter

9. Claims 60-63 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The claims include the limitation of a bus master command engine, coupled to the validator, read controller and bus, the bus master command engine initiating the command retrieval from the host memory when the bus master command engine receives a signal from the discrete host indicating host commands are available in the host memory, which is not shown by the prior art of record, in the combination as disclosed and claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri 8:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu
Examiner
Art Unit 2112

Khanh Dang
Primary Examiner

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